REMARKS

Claims 1-10, 12-15, and 27-29 are pending in this application. Claims 1, 5, 7, 9, 14, 27, and 28 have been amended. Claim 11 has been canceled. Claim 29 is new.

Section 112 Rejections

In the Office Action mailed March 25, 2005, the Examiner rejected claims 5, 7, 14, and 28 under 35 U.S.C. § 112, second paragraph, as indefinite. In particular, claim 5 was found to be unclear because of the recitation "fill polysilicon that has been enhanced by implantation." This language has been amended to delete the word "fill." Claims 7, 14, and 28 were rejected because the recitation of the first polysilicon layer having a thickness conforming to the sidewalls of the dielectric region "to prevent said region from becoming filled completely" was found to be inaccurate in that the figures show the trenches completely filled. Although the written description clearly provides support for this limitation, applicants are removing it from claims 7, 14, and 28 to further advance prosecution.

Rejections on the Merits

Claims 9-10 and 12 were rejected on 35 U.S.C. § 102(b) as anticipated by Japanese Patent No. 8-032030 ("Ando"). Claims 1, 5, 7, 11, and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over Ando in view of U.S. Patent No. 5,856,702 ("Hashimoto"). Claims 13-14 and 27-28 were rejected under 35 U.S.C. § 103(a) as unpatentable over Ando in view of U.S. Patent No. 6,054,359 ("Tsui et al."). Claims 2 and 3 were rejected as obvious over Ando and Hashimoto and further in view of U.S. Patent No. 5,753,391 ("Stone et al."). Claim 6 was rejected as obvious over Ando and Hashimoto and further in view of Tsui et al.

Applicants respectfully disagree with the bases for the rejections and request reconsideration and further examination of the claims. Ando, Japanese Patent No. 8-032030, does not teach a trench formed in a semiconductor substrate that comprises a plurality of successive or contiguous trenches of different widths formed therein.

Hashimoto, U.S. Patent No. 5,856,702, is directed to a polysilicon resistor and method of producing where a dielectric film is formed on top of a semiconductor substrate. No trench is ever formed in the substrate itself. As a result, the "slot" is not a trench because of

necessity it must be very shallow inasmuch as the dielectric formed thereon is quite thin. Moreover, Hashimoto shows the thickness of the polysilicon to be lower than the thickness of the dielectric (some hundreds of Angstroms) and thus is structurally limited and will not function as the claimed invention. In Hashimoto, the "T" shape is a normal consequence of material deposition in the narrow slots. Certain overlapping at the edges of the polysilicon must necessarily be accepted to ensure that the material can entirely fill the narrow, shallow slot. In contrast, the trench width of the present application is not so narrow and does not necessarily require that the overlapping region is formed. Moreover, in the present invention the T configuration is willingly realized to modulate the value of the layer resistance as a combination of two distinct layers, a bulk polysilicon region and a surface region.

In addition, while Hashimoto shows in Figure 6 a plurality of trenches, these trenches are not successive or contiguous to form a single trench in the substrate and they are not of different widths.

Turning to the claims, claim 1 is directed to a resistive structure integrated in a semiconductor substrate that comprises a plurality of successive trenches of different widths formed in the substrate and lined with dielectric material to form a dielectric trench. As discussed above, nowhere does Hashimoto teach or suggest such a plurality of successive trenches of different widths formed in the substrate. Rather, Hashimoto teaches forming a slot in a dielectric layer that is on top of the semiconductor substrate. Ando does not teach or suggest a plurality of successive trenches of different widths formed in the substrate.

Claim 1 further recites a polysilicon region, at least a portion of which is doped, that is surrounded by the single dielectric trench so that the resistive structure is isolated electrically from other components jointly integrated in the semiconductor substrate, wherein portions of the dielectric trench are formed with a plurality of trenches distributed to form a single dielectric region having a width that increases along the resistive structure in which a voltage drop increases. Nowhere does Ando teach or suggest the combination recited in claim 1 of a plurality of successive trenches of different widths formed in the substrate and lined with a dielectric material and filled with a polysilicon region so that the resistive structure is isolated electrically from other components, the dielectric region having a width that increases along the resistive structure in which a voltage drop increases.

Applicants respectfully submit that claim 1 and dependent claims 2-3 and 5-7 are not disclosed by Ando and are not taught or suggested by the combination of Ando and Hashimoto, the combination of Ando, Hashimoto, and Stone et al., and the combination of Ando, Hashimoto, and Tsui et al. Even if one were motivated to combine Hashimoto and Ando, the combination would fall short of the claimed combination because the plurality of Hashimoto's trenches are not of different widths and do not form a single trench of increasing width.

Independent claim 9 is directed to an integrated resistive structure that comprises at least one trench having a width that increases along a length thereof and formed in a semiconductor substrate from a plurality of successive trenches of different widths to have a depth greater than a depletion region, a dielectric layer formed of a dielectric oxide entirely coating all walls, including a bottom wall, of the at least one trench, the dielectric layer having a width that increases along a length of the at least one trench to form a fill trench of constant width, and a polysilicon region filling the fill trench to be isolated dielectrically from the semiconductor substrate, the polysilicon region having at least a portion that is doped.

As discussed above, while Hashimoto teaches a plurality of trenches, they are not successive trenches that are lined with a dielectric layer having a width that increases along a length of the at least one trench to form a fill trench of constant width. Thus, the combination of Hashimoto and Ando clearly falls short of the combination recited in claim 9. Applicants respectfully submit that claim 9 and dependent claims 10-15 are not taught or suggested by the combination of Ando and Hashimoto, and in the case of claims 13 and 14, the combination of Ando in view of Tsui et al.

Independent claim 27 recites an integrated resistive structure that comprises a trench formed in a semiconductor substrate from a plurality of contiguous trenches of different widths, a dielectric layer entirely coating all walls of the trench, the dielectric layer having a width that increases along a length of the trench to form a fill trench, and a polysilicon region comprising first and second layers of polysilicon filling the fill trench, the second layer being undoped, and the first layer implanted with a dopant. Applicants respectfully submit that claim 27 is allowable for the reasons discussed above with respect to independent claims 1 and 9. Applicants further submit that dependent claims 28 and 29 are allowable for the reasons why claim 27 is allowable.

Correction of Election of Claims

Applicants wish to bring to the Examiner's attention that in electing to prosecute the claims in the present application, applicants inadvertently designated the wrong figures. The claims as pending in this application correspond to Figure 7.

Conclusion

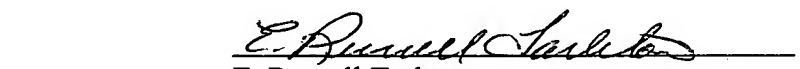
In view of the foregoing, applicants submit all of the claims in this application are now clearly in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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